PAGE 416 * RCVD AT 9/21/2006 3:34:11 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/31 * DNIS:2738300 * CSID:609 734 6888 * DURATION (mm-ss):01-12

CUSTOMER NO.: 24498 Serial No. 10/511.837

Reply to Final Office Action dated: 3/21/2006

Response dated: 9/21/2006

Atty Docket No. PU020136
RECEIVED
CENTRAL FAX CENTER

SEP 2 1 2006

CLAIM LISTING

1. (currently amended) A magnetic field compensation apparatus, comprising:

a first digital-to-analog converter responsive to a digitally encoded signal containing magnetic field compensation information; for generating a first analog signal containing the magnetic field compensation information from said digitally encoded signal;

a magnetic field compensation winding positioned on a cathode ray tube; an amplifier responsive to said first analog signal and having an output that is coupled to said magnetic field compensation winding for producing a current in said magnetic field compensation winding, said current producing a magnetic field in a beam path of said cathode ray tube that compensates for an ambient magnetic field; and

a second digital-to-analog converter for generating a second analog signal that is coupled to an input of said amplifier that varies said current in accordance with said second analog signal;

wherein said compensation winding is coupled to a source of a supply voltage, wherein a polarity of said current varies in accordance with a difference between an output voltage of said amplifier and said supply voltage and wherein a polarity of said amplifier output voltage remains the same both when said current is at a first polarity and when said current is at a polarity that is opposite to said first polarity.

- 2. (original) The apparatus according to Claim 1, wherein said second analog signal tracks variations in said first analog signal for providing error compensation and wherein said magnetic field compensation current is controlled in accordance with a difference between said first and second analog signals.
- 3. (original) The apparatus according to Claim 1, wherein said digital-to-analog converters are separate units contained in a single integrated circuit.
- 4. (original) The apparatus according to Claim 1, wherein said digital-to-analog converters are energized from a common supply voltage.

PACE 5/6 * RCVD AT 9/21/2006 3:34:11 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/31 * DNIS:2738300 * CSID:609 734 6888 * DURATION (mm-ss):01-12

CUSTOMER NO.: 24498

Atty Docket No. PU020136

Serial No. 10/511,837

Reply to Final Office Action dated: 3/21/2006

Response dated: 9/21/2006

- 5. (original) The apparatus according to Claim 1, wherein said amplifier comprises a differential, input stage, wherein said first analog signal is coupled to one of an inverting input and a non-inverting input of said amplifier and wherein said second analog signal is coupled to the other one of said inverting and non-inverting inputs of said amplifier.
- 6. (cancel)
- 7. (original) The apparatus according to Claim 1, further comprising a current negative feedback path coupled to said amplifier to reduce a dependency of said current on an impedance of said winding.

8-12. (cancel)

- 13. (new) A magnetic field compensation apparatus, comprising:
- a first digital-to-analog converter responsive to a digitally encoded signal containing magnetic field compensation information; for generating a first analog signal containing the magnetic field compensation information from said digitally encoded signal;
- a magnetic field compensation winding positioned on a cathode ray tube; an amplifier responsive to said first analog signal and having an output that is coupled to said magnetic field compensation winding for producing a current in said magnetic field compensation winding, said current producing a magnetic field in a beam path of said cathode ray tube that compensates for an ambient magnetic field;
- a second digital-to-analog converter for generating a second analog signal that is coupled to an input of said amplifier that varies said current in accordance with said second analog signal;
- a source of a second digitally encoded signal coupled to an input of said second digital-to-analog converter, wherein, during a degaussing interval, said value of said first and second digitally encoded signals are made to be equal for preventing the generation of said current.